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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,432	09/30/2003	Allen Bruce Goodrich	1001.29	6197

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EXAMINER	
DARE, RYAN A	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,432	GOODRICH, ALLEN BRUCE	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

RD

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Flautner et al., US Patent Application Publication 2004/0210728.

3. With respect to claim 1, Flautner et al. teach a method of reducing power consumption in a multi-way set associative cache memory, comprising:

During a first clock cycle, in response to an address, identifying an associated set in the cache memory, comparing the address to respective tag potions of blocks in the associated set, and outputting a signal in response thereto, in par. 0103 and par. 0105, with reference to fig. 9, where numeral 900 is the address, the index field 914 identifies the associated set in the cache memory, the address is compared to numeral 950 or 952 in the Tag RAM 930 or Tag RAM 932, respectively, and the output of MATCH unit 954 or 956 indicates a match; and

During a second clock cycle, in response to the signal indicating a match between one of the blocks and the address, reading a non-tag portion of the matching

block in the associated set, while a non-matching block in the associated set is disabled, in figure 10, where in response to a match in numeral 1020, data is read in numeral 1030 and the non-matching block is disabled in numeral 1060. Note, with reference to the specification, paragraphs 0106 and 0109, that this is the alternative embodiment where the tag portion is also disabled when not in use. In the primary embodiment, as with the present invention, where the tags are always awake and readable, numerals 1040 and 1050 of the process can be eliminated, and the unneeded lines can be set back into drowsy mode after reading the matching data.

4. With respect to claim 2, Flautner et al. teach the method of claim 1, wherein the reading comprises: enabling the non-tag portion of the matching block in the associated set, in fig. 0105, "If a match is found then the CPU is signaled to load the requested data from the appropriate cache line. Data is supplied to the CPU from the data RAM 940 via multiplexer 960." See the abstract where it describes that when data is read, it is enabled by raising the voltage level to a readable state. Also see the first sentence of par. 0106 which says that in the primary embodiment, the tag line is always enabled, which means that the non-tag portion is the part that is enabled for reading.

5. With respect to claim 3, Flautner et al. teach the method of claim 2, wherein the enabling comprises applying power to the non-tag portion of the matching block in the associated set, in the abstract where it describes that when data is read, it is enabled by raising the voltage level to a readable state.

6. With respect to claim 4, Flautner et al. teach the method of claim 1, and comprising: removing power from the non-matching block in the associated set, in figure

10, numeral 1060, and further described by the abstract, wherein the drowsy mode refers to the unreadable lower voltage level.

7. With respect to claim 5, Flautner et al. teach the method of claim 4, wherein removing the power comprises:

removing power from the non-matching block in the associated set, so that the non-matching block in the associated set is disabled from outputting information, and so that the non-matching block in the associated set continues to store the information, in the abstract.

8. With respect to claim 6, Flautner et al. teach the method of claim 1, wherein the cache memory is a program cache, in par. 0122, where it mentions an instruction cache, which is synonymous with program cache.

9. With respect to claim 7, Flautner et al. teach the method of claim 1, wherein the cache memory is a data cache, in par. 0122.

10. With respect to claim 8, Flautner et al. teach the method of claim 1, wherein comparing the address comprises: comparing a portion of the address to respective tag portions of blocks in the associated set, in par. 0103.

11. With respect to claim 9, Flautner et al. teach the method of claim 1, wherein reading the non-tag portion comprises: reading the non-tag portion of the matching block in the associated set, in fig. 10, numeral 1030, while the non-matching block in the associated set is at least partly disabled, in fig. 10, numeral 1060.

12. With respect to claim 10, Flautner et al. teach the method of claim 1, wherein reading the non-tag portion comprises: reading the non-tag portion of the matching

block in the associated set, in fig. 10, numeral 1030, while at least first and second non-matching blocks in the associated blocks in the associated set are disabled, in fig. 10, numeral 1060.

13. With respect to claim 11, Flautner et al. teach a system for reducing power consumption in a multi-way set associative cache memory, comprising:

first circuitry for: during a first clock cycle, in response to an address, identifying an associated set in the cache memory, comparing the address to respective tag potions of blocks in the associated set, and outputting a signal in response thereto, in par. 0103 and par. 0105, with reference to fig. 9, where numeral 900 is the address, the index field 914 identifies the associated set in the cache memory, the address is compared to numeral 950 or 952 in the Tag RAM 930 or Tag RAM 932, respectively, and the output of MATCH unit 954 or 956 indicates a match; and

second circuitry for: during a second clock cycle, in response to the signal indicating a match between one of the blocks and the address, reading a non-tag portion of the matching block in the associated set, while a non-matching block in the associated set is disabled, in the dynamic voltage scaling circuit of fig. 2 and fig. 4, and described in figure 10, where in response to a match in numeral 1020, data is read in numeral 1030 and the non-matching block is disabled in numeral 1060. Note, with reference to the specification, paragraphs 0106 and 0109, that this is the alternative embodiment where the tag portion is also disabled when not in use. In the primary embodiment, as with the present invention, where the tags are always awake and

readable, numerals 1040 and 1050 of the process can be eliminated, and the unneeded lines can be set back into drowsy mode after reading the matching data.

14. With respect to claim 12, Flautner et al. teach the system of claim 11, wherein the second circuitry is for enabling the non-tag portion of the matching block in the associated set, in fig. 0105, "If a match is found then the CPU is signaled to load the requested data from the appropriate cache line. Data is supplied to the CPU from the data RAM 940 via multiplexer 960." See the abstract where it describes that when data is read, it is enabled by raising the voltage level to a readable state. Also see the first sentence of par. 0106 which says that in the primary embodiment, the tag line is always enabled, which means that the non-tag portion is the part that is enabled for reading.

15. With respect to claim 13, Flautner et al. teach the system of claim 12, wherein the second circuitry is for applying power to the non-tag portion of the matching block in the associated set, in the abstract where it describes that when data is read, it is enabled by raising the voltage level to a readable state.

16. With respect to claim 14, Flautner et al. teach the system of claim 11, wherein the second circuitry is for removing power from the non-matching block in the associated set, in figure 10, numeral 1060, and further described by the abstract, wherein the drowsy mode refers to the unreadable lower voltage level.

17. With respect to claim 15, Flautner et al. teach the system of claim 14, wherein the second circuitry is for removing power from the non-matching block in the associated set, so that the non-matching block in the associated set is disabled from

outputting information, and so that the non-matching block in the associated set continues to store the information, in the abstract.

18. With respect to claim 16, Flautner et al. teach the system of claim 11, wherein the cache memory is a program cache, in par. 0122, where it mentions an instruction cache, which is synonymous with program cache.

19. With respect to claim 17, Flautner et al. teach the system of claim 11, wherein the cache memory is a data cache, in par. 0122.

20. With respect to claim 18, Flautner et al. teach the system of claim 11, wherein the first circuitry is for comparing a portion of the address to respective tag portions of blocks in the associated set, in par. 0103.

21. With respect to claim 19, Flautner et al. teach the system of claim 11, wherein the second circuitry is for reading the non-tag portion of the matching block in the associated set, in fig. 10, numeral 1030, while the non-matching block in the associated set is at least partly disabled, in fig. 10, numeral 1060.

22. With respect to claim 20, Flautner et al. teach the system of claim 11, wherein the second circuitry is for reading the non-tag portion of the matching block in the associated set, in fig. 10, numeral 1030, while at least first and second non-matching blocks in the associated blocks in the associated set are disabled, in fig. 10, numeral 1060.

Conclusion

23. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar methods and systems of reducing power consumption in cache memory.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan Dare
October 13, 2005

MATTHEW C. ANDERSON
PRIMARY EXAMINER